SiT8021 Preliminary
Ultra-Small, 1 to 26 MHz Oscillator

SiTime
The Smart Timing Choice™

Description

The SiT8021is the industry's smallest and the lowest power MHz oscillator. With 0.1 mW of active power consumption at 3.072 MHz output frequency, this µPower oscillator enables longer battery life for a wearable, IoT or mobile device comparing to a quartz based oscillator or resonator.

The device comes in the smallest 1.5 mm x 0.8 mm package. The unique combination of ultra-low power, ultra-small package and flexible output frequency makes it ideal for power sensitive and space constrained applications including:

- Tablets
- Fitness bands
- Health and medical monitoring
- Wearables
- Portable audio
- Input devices
- IoT devices

Features

- Ultra-low current consumption of 60 µA at 3.072 MHz
- Ultra-small 1.5 mm x 0.8 mm package
- 1 to 26 MHz with 6 decimal places of accuracy
- Operating temperature from -40°C to 85°C
- Programmable output drive strength for best EMI or driving multiple loads
- Ultra-light weight of 1.28 mg
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

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TempFlat MEMS™

Electrical Specifications

Table 1. Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	1.000000		26.000000	MHz	
Frequency Stability and Aging						
Initial Tolerance	f_tol	-10	–	+10	ppm	Frequency offset at 25°C
Frequency Stability	f_stab	-100	–	+100	ppm	Inclusive of initial tolerance, and variations over operating temperature, rated power supply voltage and output load. Contact SiTime for ±25 or ±50 ppm over -20 to 70°C.
First Year Aging	f_1year	-3		+3	ppm	at 25°C
Operating Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage and Current Consumption						
Supply Voltage	VDD	1.62	1.8	1.98	V	
Current Consumption[1]	IDD	–	60	–	µA	f = 3.072 MHz, No load
		–	119	150	µA	f = 6.144 MHz, No load
		–	230	270	µA	f = 6.144 MHz, 10 pF load
		–	228	–	µA	f = 12 MHz, No load
Standby Current	I_std	–	0.9	2	µA	ST pin = HIGH, Output is weakly pulled down
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	T_r, T_f	–	–	8	ns	20% - 80%. Contact SiTime for other programmable rise/fall options
Output High Voltage	VOH	90%	–	–	VDD	IOH = -0.5 mA
Output Low Voltage	VOL	–	–	10%	VDD	IOL = 0.5 mA
Input Characteristics						
Input High Voltage	VIH	75%	–	–	VDD	
Input Low Voltage	VIL	–	–	25%	VDD	
Input Slew Rate	In-slew	10	–	–	V/µs	
Input Pull-down Impedence	Z_in	200	–	–	kΩ	Active mode (ST pin = LOW)
		3	–	–	MΩ	Standby mode (ST pin = HIGH)
Input Capacitance	C_in	–	–	7	pF	

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Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Startup, Standby and Resume Timing						
Startup Time	T_start	–	150	500	ms	Measured from the time VDD reaches 90% of its final value
Standby Time	T_stdby	–	–	20	µs	
Resume Time	T_resume	–	2.5	5	ms	Measured from the time ST pin crosses 50% threshold
Jitter						
RMS Period Jitter	T_jitt	–	90	140	ps	f = 6.144 MHz
RMS Phase Jitter	T_phj	–	1.3	2.5	ns	f = 6.144 MHz, Integration bandwidth = 100 Hz to 40 kHz. Inclusive of 50 mV peak-to-peak sinusoidal noise on Vdd. Noise frequency 100 Hz to 20 MHz.

Note:

1. Current consumption with load is a function of the output frequency and output load. For any given output frequency, the capacitive loading will increase current consumption equal to C_load*VDD*f(MHz).

Table 2. Pin Description

Pin	Symbol	Functionality	
1	ST	Input	L: Specified frequency output H: Output is low (weak pull down). Device goes to the standby mode. Supply current reduces to I_std.
2	OUT	Output	LVCMOS clock output
3	VDD	Power	Supply voltage. Bypass with a 0.01µF X7R capacitor.
4	GND	Power	Connect to ground

Top View

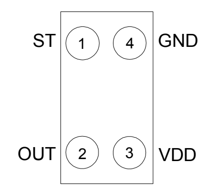


Figure 1. Pin Assignments

Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Condition	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 3.63	V
Short Duration Maximum Power Supply Voltage (Vdd)	<30 seconds	4.0	V
Continuous Maximum Operating Temperature Range		105	°C
Short Duration Maximum Operating Temperature Range	≤30 seconds	125	°C
Human Body Model (HBM) ESD Protection	JESD22-A115	2000	V
Charge-Device Model (CDM) ESD Protection	JESD22-C101	750	V
Machine Model (MM) ESD Protection	T_A = 25°C	200	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Sock Resistance	Mil 883, Method 2002	10	kg
Mechanical Vibration Resistance	Mil 883, Method 2007	70	g
1508 CSP Junction Temperature		150	°C
Storage Temperature		-65 to 150	°C
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Block Diagram

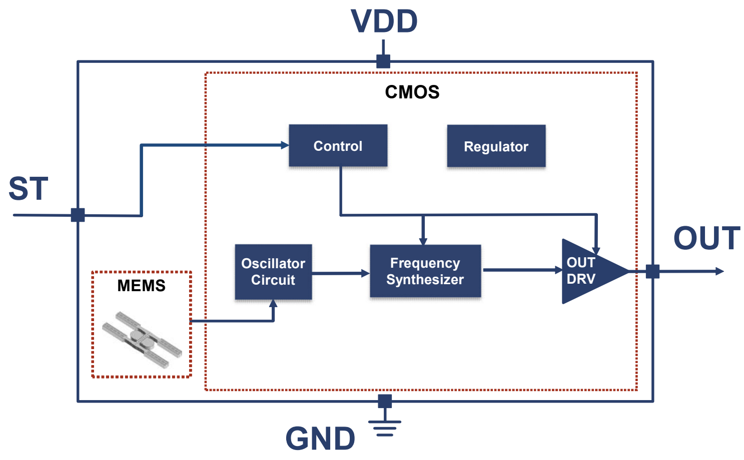


Figure 2

Device Operating Modes and Outputs

The SiT8021 supports ≤0.9 µA standby mode for battery-powered and other power sensitive applications. The switching between the active and standby modes is controlled by the logic level on the ST pin as shown in the table below.

Table 4. Operating Modes and Output States

ST Pin	MODE	OUTPUT	Max IDD Example
LOW	Active	Specified frequency	60 µA @ 3.072 MHz
FLOAT	Active with 200 kΩ internal pull-down	Specified frequency	60 µA @ 3.072 MHz
HIGH	Standby	Hi-Z, pulled-down with 1 MΩ impedence	2 µA

Active Mode

The SiT8021 operates in the active mode when the ST pin is at logic LOW or FLOAT. In the active mode, the device uses the on-chip frequency synthesizer to generate an output from the internal MEMS resonator reference. The frequency of the output is factory programmed based on the device ordering code.

Standby Mode

The SiT8021 operates in the standby mode when the ST pin is at logic HIGH. In the standby mode, all internal circuits with the exception of the MEMS oscillator circuit and the ST pin detection logic are turned off to reduce power consumption. While in standby mode, the input impedance of the ST pin is increased to further reduce system level power consumption.

The output driver of the device in the standby mode is pulled-down with 1 MΩ.

Output During Startup and Resume

The SiT8021 starts up with the output disabled. The output is enabled once all internal circuit blocks are active, and logic LOW or FLOAT is detected on the ST pin.

As shown in Table 4, logic HIGH at ST pin forces the SiT8021 into “standby” state, causing the output to disable. Upon pulling ST pin LOW, the device enters “resume” state, keeping the output disabled. Once “resume” state ends, the device output enables.

The first clock pulse after startup or resume is accurate to the rated stability.

Low Power Design Guidelines

For high EM noise environments, we recommend the following design guidelines:

- Place oscillator as far away from EM noise sources as possible (e.g., high-voltage switching regulators, motor drive control).
- Route noisy PCB traces, such as digital data lines or high di/dt power supply lines, away from the SiTime oscillator.
- Place a solid GND plane underneath the SiTime oscillator to shield the oscillator from noisy traces on the other board layers.

Manufacturing Guidelines

- No Ultrasonic or Megasonic Cleaning: Do not subject the SiT8021 to an ultrasonic or megasonic cleaning environment. Permanent damage or long term reliability issues to the device may occur in such an event.
- Applying board-level underfill (BLUF) to the device is acceptable, but will cause a slight shift of few PPM in the initial frequency tolerance. Tested with UF3810, UF3808, and FP4530 underfill.
- Reflow profile, per JESD22-A113D.
- For additional manufacturing guidelines and marking/ tape-reel instructions, click on the following link: http://www.sitime.com/component/docman/doc_download /243-manufactuing-notes-for-sitime-oscillators

Test Circuit and Waveform

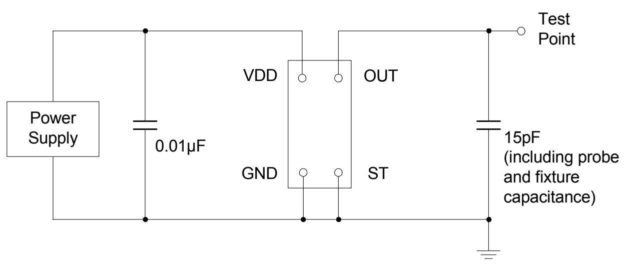


Figure 3. Test Circuit

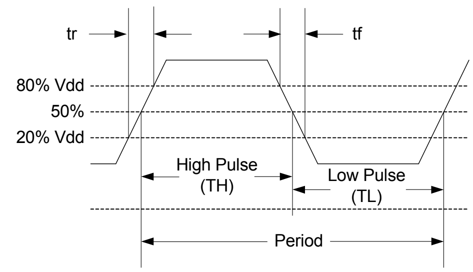


Figure 4. Waveform[1]

Note:

2. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagram

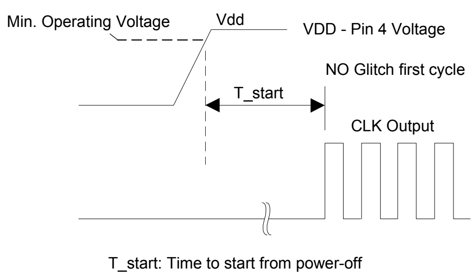


Figure 5. Startup Timing

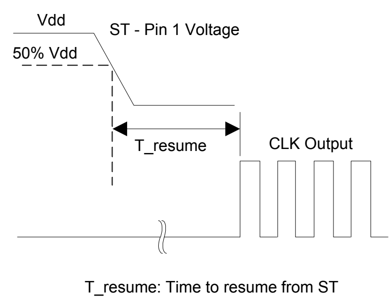


Figure 6. Resume Timing

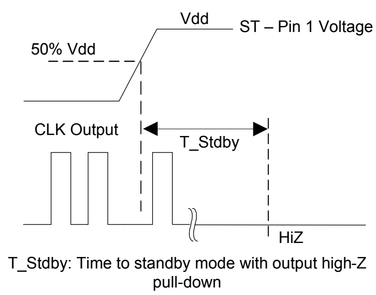


Figure 7. Standby Timing

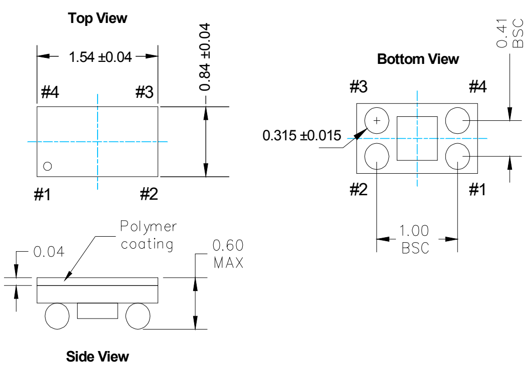
Notes:

3. SiT8021 supports “no runt” pulses and “no glitch” output during startup or resume.
4. SiT8021 supports gated output which is accurate within rated frequency stability from the first cycle.

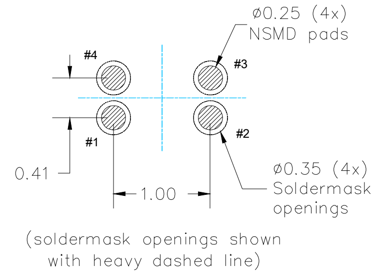
Dimensions and Patterns

Package Size – Dimensions (Unit: mm)

1.55 x 0.85 mm CSP



Recommended Land Pattern (Unit: mm)



Recommend 4-mil (0.1mm) stencil thickness

Ordering Information

SiT8021AC-J4-18S-6.144000D

Part Family
"SiT8021"

Revision Letter
"A" is the revision

Temperature Range
"C" Commercial, -20 to 70ºC
"I" Industrial, -40 to 85ºC

Output Drive Strength[5]
"–" Default

Package Size
"J" 1.5 x 0.8 mm x mm

Frequency Stability
"4" for ±100 ppm

Supply Voltage
"18" for 1.8V ±10%

Feature Pin
"S" for Standby

Frequency
1.000000 to 26.000000 MHz

Packaging
"D": 8 mm Tape & Reel, 3ku reel
"E": 8 mm Tape & Reel, 1ku reel
"S": 8 mm Tape & Reel, 10ku reel

Note:

5. Contact SiTime for other drive strength options that result in different rise/fall time for any given output load.

Revision History

Table 6. Datasheet Version and Change Log

Version	Release Date	Change Summary
0.1	12/15/14	Advance Information
0.2	1/27/15	• Updated CSP dimension tolerance • Removed 2.0 mm x 1.6 mm package • Changed to 6.144 MHz as the reference frequency for jitter, IDD and other relevant parameters • Changed resume time (max) to 5 ms • Changed the parameter PSNR to Power Supply Noise Sensitivity and specified in RMS
0.3	3/31/15	• Changed VIL and VIH values in the EC table • Reduced standby time in the EC table • Revised phase jitter condition to include power supply noise sensitivity • Removed power supply noise spec
0.9	5/22/15	• Added typical values for active and standby current • Added current consumption for additional frequencies • Changed ±50 ppm option to Contact SiTime • Added manufacturing guideline • Other miscellaneous format and footnote changes